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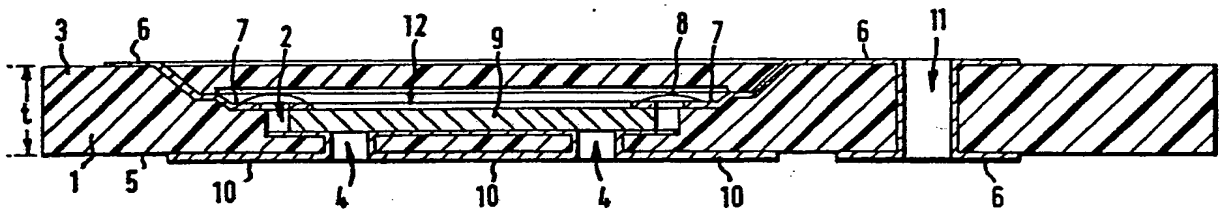
(54) Title: MOUNTING SEMI-CONDUCTOR CHIPS



(57) Abstract

An electronic circuit mount (1), for semi-conductor chips, has a series of closed-bottomed recesses (2) within the thickness (t) of the mount, with each recess opening to a surface (3) of the mount and being shaped to house a semi-conductor chip (9) of given configuration; the amount having an applied pattern (6) of chip-interconnecting electrical conductors (7) extending over the mount and to each recess: the mount being moulded from thermoplastic material and each recess having means (4, 10) for conducting away and dissipating heat therefrom. In use, the heat conducting and dissipating means convey heat generated by a chip away from the recess it is mounted in and prevents the thermoplastic of the mount in the area of the recess from degrading.

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MOUNTING SEMI-CONDUCTOR CHIPS

This invention relates to mounting semi-conductor chips, such as integrated circuit dies or discrete components on an electronic circuit mount such as a circuit or wiring board to form an electronic sub-assembly.

Conventional printed circuit boards are formed of a thin board (of between 0.0127 mm and 32 mm thickness) with a conducting interconnection pattern formed on one or both faces of the board; feedthroughs and vias being provided to connect the interconnection patterns on either face of the board and for wires or leads from discrete components, semi-conductor chips and integrated circuit dies that are often mounted on carriers which are then added to complete the circuit for the thus formed sub-assembly. Printed circuits have also been produced with several alternating layers of metal film and insulating film mounted on a single board; boards with up to 32 layers of interconnections have been produced. Such multi-layer boards have enhanced components/chips/die packing densities and reduced interconnection lengths resulting in higher operating speeds for the sub-assembly.

United Kingdom Patent Specification No.953503 (Telefunken) describes the mounting of an active circuit element in a recess at one side of a carrier plate of

insulating material, the only insulating material disclosed being ceramic material. United Kingdom Patent Specification No.2026234A (Mitsumi) also describes the accommodation of a circuit element chip within a concavity or depression in a ceramic substrate, the use of substrate materials other than ceramic is contra-indicated by the disclosure of this specification (see page 1 lines 31 to 34).

It is an object of the present invention to provide an electronic circuit mount having recesses to house semi-conductor chips and moulded from thermoplastic material. Such materials have the advantages of being easily moulded, inexpensive and, for high frequency operations, improved dielectric characteristics. However, the drawback to the use of thermoplastic material is its ease of thermal degradation and it is a further object of the present invention to overcome this defect.

According to the present invention, an electronic circuit mount, for semi-conductor chips, has a series of closed-bottomed recesses within the thickness of the mount, with each recess opening to a surface of the mount and being shaped to house a semi-conductor chip of given configuration; the mount having an applied pattern of chip-interconnecting electrical conductors extending over the mount and to each recess; the

mount being moulded from thermoplastic material and each recess having means for conducting away and dissipating heat therefrom. In use, the heat conducting and dissipating means convey heat generated by a chip away from the recess it is mounted in and prevents the thermoplastic of the mount in the area of the recess from degrading.

In an embodiment of the present invention, the heat conducting and dissipating means comprise one or more thermal vias extending from each recess to another surface of the mount.

In a further embodiment of the present invention, the heat conducting and dissipating means further comprise an applied thermal conducting layer extending over part of each recess, the or each thermal via and a part of said other surface of the mount. By this means, a chip attached, such as by bonding, to the thermal conducting layer in a recess has the heat it generates conducted away through the thermal via and radiated from the layer on said other surface.

In a preferred embodiment of the present invention, the mount is a circuit board, the recesses each open to one of the opposed faces of the board, the thermal vias extend from the bottom of each recess to the opposite board face and the thermal conducting layer

extends over the bottom of each recess.

Conveniently, the pattern of electrical conductors and the thermal conducting layer are simultaneously applied to the mount by a process of selective metalisation.

A cover for each recess may be provided in the form of a lid moulded from thermoplastic material and shaped to fit the sides of the recess and to be flush with the mount surface.

The above and other features of the present invention are illustrated, by way of example, by the Drawing of a section through an electronic circuit mount in accordance with the invention but showing only one recess.

As shown a board 1 has a recess 2 in one face 3 thereof; as shown the recess is within the thickness of the board (in an example the thickness is 1.6 mm).

Thermal vias or holes 4 are provided in the bottom of the recess 2, which vias emerge on the opposite face 5 of the board. The board is provided with an applied pattern 6 of chip-interconnecting electrical conductors that covers face 3 of the board and extends down into the recess 2 to provide wiring connection points 7 for the electrical connection of wiring-leads 8 to a semi-conductor chip 9, such as an integrated circuit die that is housed in the recess.

The bottom of the recess, the thermal vias 4 and a part of the opposite face 5 of the board are covered with a thermal conducting layer 10 the chip 9 being bonded, such as by a thermally conductive adhesive, to the layer in the recess bottom. The thermal vias 4 and conducting layer 10 serve to conduct heat from the semi-conductor chip 9 to the thermal coating on the other side of the board which forms a spreader plane to radiate the heat generated in the semi-conductor device.

Feedthroughs for the board 10 are provided in the form of vias 11 from one to the other sides of the board through which vias the conducting pattern 6 can extend.

The recess 2 is covered by a lid 12 that is shaped to fit the sides of the recess and be essentially flush with the surface of the board face 3. Additionally, the remaining free space 13 within the recess can be filled with an insulating material, such as an epoxy resin to "pot" the chip in the device both to anchor it therein and provide additional protection beyond that provided by the lid 12.

The board may be formed using high performance thermoplastic materials either filled or unfilled, of the type polyethersulphone, polysulphone, polyetherimide, polyphenylene sulphide or the like and may be produced

by injection moulding or any other suitable technique. The electrical conducting interconnection pattern 6 is then produced on the board sides and into the recess by selective metallisation. The thermal conducting layer 10 is also formed by selective metallisation, preferably by the same operation as that forming the electrical conducting pattern 6.

The lid 12 can be similarly formed and from similar materials and is adhesively bonded or welded into place, after filling any free space within the recess with an epoxy resin potting compound.

More than one recess is provided on each board to mount further semi-conductor chips or devices and further chips or devices may be surface mounted or through hole mounted on to the board to provide a complete electronic sub-assembly that can be functionally tested before further assembly.

The composite structure of the thus formed electronic sub-assembly will operate at much higher speeds than conventionally packaged and interconnected systems due to the short interconnection lengths possible and the low dielectric constant of the materials used; whilst the thermal conduction means prevents the board from overheating in the area of each recess, to the detriment of both the chip and the board thermoplastic material.

CLAIMS:

1. An electronic circuit mount, for semi-conductor chips, having a series of closed-bottomed recesses within the thickness of the mount, each recess opening to a surface of the mount and being shaped to house a semi-conductor chip of given configuration; the mount having an applied pattern of chip-interconnecting electrical conductors extending over the mount and to each recess characterised in that the mount is moulded from thermoplastic material and each recess has means for conducting away and dissipating heat therefrom.

2. A mount as claimed in claim 1, and characterised in that said heat conducting and dissipating means comprise one or more thermal vias extending from each recess to another surface of the mount.

3. A mount as claimed in claim 2, and characterised in that said heat conducting and dissipating means further comprise an applied thermal conducting layer extending over part of each recess, the or each thermal via and a part of said other surface of the mount.

4. A mount as claimed in claim 3, and characterised in that the mount is a circuit board, the recesses each open to one of the opposed faces of the board, the thermal vias extend from the bottom of each recess to the opposite board face and the thermal conducting layer

extends over the bottom of each recess.

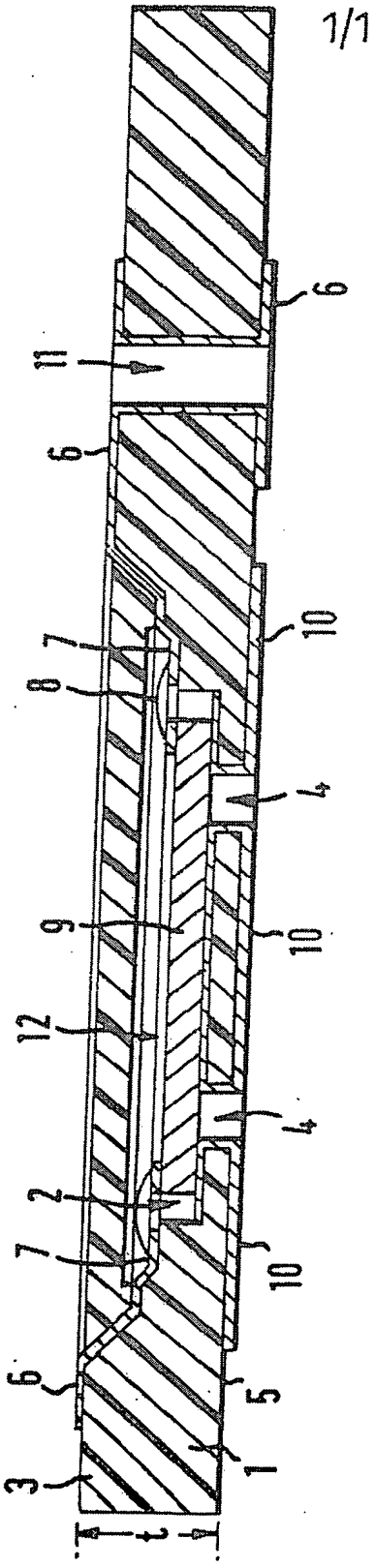
5. A mount as claimed in claim 3 or claim 4, and characterised in that the pattern of electrical conductors and the thermal conducting layer are simultaneously applied to the mount.

6. A mount as claimed in claim 3 or claim 4, and characterised in that the pattern of electrical conductors and the thermal conducting layer are both formed by selective metallisation of the mount.

7. A mount as claimed in any of claims 1 to 6, and characterised in that the thermoplastic material is a high performance thermoplastic selected from the group polyethersulphone, polysulphone, polyetherimide, polyphenylene sulphide.

8. A mount as claimed in any of claims 1 to 7, and characterised in that means are attached to the mount to cover each recess.

9. A mount as claimed in claim 8 and characterised in that each said cover means is a lid moulded from thermoplastic material and shaped to fit the sides of the recess and to be flush with the mount surface.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INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 85/00196

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 01 L 23/12; H 01 L 23/14; H 01 L 23/36; H 01 L 23/48

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 01 L

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	EP, A, 0072673 (MINNESOTA MINING & MANUFACTURING COMP.) 23 February 1983, see figure 1, page 7, lines 7-12	1
A	--	4,7
Y	US, A, 3777220 (IBM) 4 December 1973, see figure 5; claims 1,13; column 5, lines 20-31	1
A	--	2,4,8
A	EP, A, 0055578 (HONEYWELL) 7 July 1982, see figure 1; claim 1; page 4, lines 20-22; page 5, lines 2-9; page 5, line 19-page 6, line 1	1-6
A	-- DE, A, 2546443 (SIEMENS) 21 April 1977, see figure 2; claims 1,5	9
A	-- Patent Abstracts of Japan, volume 7, nr. 45, (E-160) (1190) 23 February 1983, & JP, A, 57196548 (TOKYO SHIBAURA) 2 December 1982	8

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* Special categories of cited documents: [10]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
29th July 1985	20 AOUT 1985
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	G.L.M. Kruydenberg

Form PCT/ISA/210 (second sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/GB 85/00196 (SA 9582)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 09/08/85

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A- 0072673	23/02/83	JP-A-	58039048	07/03/83
		US-A-	4472876	25/09/84
US-A- 3777220	04/12/73	FR-A,B	2191406	01/02/74
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		CA-A-	1167571	15/05/84
		AU-B-	545035	27/06/85
DE-A- 2546443	21/04/77	None		

For more details about this annex :
see Official Journal of the European Patent Office, No. 12/82